CLAIMS

What is claimed is:

1. A resistor comprising an ion implanted resistor formed in a crystalline silicon substrate of the opposite conductivity type, the resistor being isolated from the rest of the substrate by a PN junction and having an implantation dose providing a minimum resistance at a temperature of approximately room temperature.

2. The resistor of claim 1 wherein the silicon substrate is a p-type substrate and the resistor body is formed by arsenic implantation.

3. The resistor of claim 1 wherein the temperature variation of the resistance of the resistor across the temperature range of -40C to +85C is less than 3%.

4. The resistor of claim 1 further comprising first and second heavily doped regions of the same conductivity type as the resistor body providing first and second contacts to the resistor.

5. The resistor of claim 4 further comprising an insulating layer over the resistor with contact openings therein to provide access to the first and second heavily

doped regions, and a patterned metal layer there over providing electrical contact to the heavily doped regions.

6. The resistor of claim 1 wherein the resistor comprises part of a CMOS integrated circuit.

7. The resistor of claim 1 wherein the resistor comprises part of a bipolar integrated circuit.

8. An integrated circuit on a crystalline silicon substrate of a first conductivity type for operating over a temperature range of T_1 to T_2, including an ion implanted resistor formed in the crystalline silicon substrate of the opposite conductivity type, the resistor being isolated from the rest of the substrate by a PN junction and having an implantation dose providing a minimum resistance at a temperature of approximately $(T_1 + T_2)/2$.

9. The integrated circuit of claim 8 wherein the silicon substrate is a p-type substrate and the resistor body is formed by arsenic implantation.

10. The integrated circuit of claim 9 wherein the temperature T_1 is -40C and T_2 is +85C.

11. The integrated circuit of claim 8 further comprising first and second heavily doped regions of the same

conductivity type as the resistor body providing first and second contacts to the resistor.

12. The integrated circuit of claim 11 further comprising an insulating layer over the resistor with contact openings therein to provide access to the first and second heavily doped regions, and a patterned metal layer there over providing electrical contact to the heavily doped regions.

13. The integrated circuit of claim 8 wherein the integrated circuit is a CMOS integrated circuit.

14. The integrated circuit of claim 8 wherein the integrated circuit comprises a bipolar integrated circuit.

15. The integrated circuit of claim 8 wherein the minimum resistance is within 20C of the temperature of $(T_1 + T_2)/2$.

16. The integrated circuit of claim 8 wherein the minimum resistance is within 10C of the temperature of $(T_1 + T_2)/2$.

17. The integrated circuit of claim 8 wherein the minimum resistance is within 5C of the temperature of $(T_1 + T_2)/2$.

18. The integrated circuit of claim 8 wherein the resistances of the resistor at the two temperature extremes are within 1% of each other.

19. The integrated circuit of claim 8 wherein the resistances of the resistor at the two temperature extremes are within 0.5% of each other.

20. The integrated circuit of claim 8 wherein the resistances of the resistor at the two temperature extremes are within 0.25% of each other.

21. A method of forming a resistor on a crystalline silicon substrate in an integrated circuit intended to operate over a temperature range of T_1 to T2 comprising:

before a final high temperature exposure associated with the processing of the active devices of the integrated circuit, forming a resistor of one conductivity type in the crystalline silicon substrate of an opposite conductivity type by ion implantation, the resistor being isolated from the rest of the substrate by a PN junction, using an implantation dose providing, in the completed integrated circuit, a minimum resistance at a temperature of approximately $(T_1 + T_2)/2$.

22. The method of claim 21 wherein the silicon substrate is a p-type substrate and the resistor body is formed by arsenic implantation.

23. The method of claim 22 wherein the temperature T_1 is -40C and T_2 is +85C.

24. The method of claim 22 further comprising forming first and second heavily doped regions of the same conductivity type as the resistor body to provide first and second contacts to the resistor.

25. The method of claim 24 further comprising forming an insulating layer over the resistor with contact openings therein to provide access to the first and second heavily doped regions, and providing a patterned metal layer there over to provide electrical contact to the heavily doped regions.

26. The method of claim 21 wherein the integrated circuit is a CMOS integrated circuit.

27. The method of claim 21 wherein the integrated circuit comprises a bipolar integrated circuit.

28. The method of claim 21 wherein the minimum resistance is within 20C of the temperature of $(T_1 + T_2)/2$.

29. The method of claim 21 wherein the minimum resistance is within 10C of the temperature of $(T_1 + T_2)/2$.

30. The method of claim 21 wherein the minimum resistance is within 5C of the temperature of $(T_1 + T_2)/2$.

31. The method of claim 21 wherein the resistance values of the resistor at the two temperature extremes are within 1% of each other.

32. The method of claim 21 wherein the resistance values of the resistor at the two temperature extremes are within 0.5% of each other.

33. The method of claim 21 wherein the resistance values of the resistor at the two temperature extremes are within 0.25% of each other.